AMENDMENTS TO THE CLAIMS:

Please enter this Amendment found in this listing of claims to replace all prior versions, and listings of claims in the application.

LISTING OF CLAIMS:

What is claimed is:

1 1. (Cancelled)

2. (Currently Amended) ~~The~~ A circuit for use in a microprocessor, comprising a 4-2 compressor circuit ~~having~~ which includes a full adder ~~formed with a XOR/XNOR cell~~, said full adder providing a Carry out, a Sum and a complementary sum output signal, and including a first and one other instance of ~~said~~ XOR/XNOR cells and two pass-logic 2-1 multiplexors, each of said multiplexors being coupled ~~to said full adder and to said one other instance of~~ said XOR/XNOR cells.

3. (Currently Amended) The circuit according to claim 2 wherein the 4-2 compressor circuit with a full adder and XOR/XNOR cells is connected by having ~~its~~ three input bits (Fig. 4, X, Y and Z) of said 4-2 compressor circuit passed into the full adder, which full adder generates said Carry out signal as a first order carry out (Cout), and said intermediate sum (S), and said intermediate complementary sum (S') and having last input bits (W and Cin) passed into a further third ~~said one other~~ instance of said XOR/XNOR cells.

4. (Currently Amended) The circuit according to claim 3 wherein said last input bits (W and Cin) are passed into said ~~one other~~ further third instance of said XOR/XNOR cells and generate an intermediate XOR signal (I) and an intermediate XNOR signal (I').

5. (Previously Amended) The circuit according to claim 4 wherein a complementary sum (S') and an intermediate sum (S) are passed into one of the 2-1 MUXs using said intermediate XOR signal (I) as a control signal and wherein the output of said one of the 2-1 MUXs is (10) the final sum Sum) and said complementary sum (S') and a carry-in bit (Cin) are passed into another of said 2-1 MUXs.

6. (Original) The circuit according to claim 5 wherein said intermediate XNOR is used as the control signal and a (11) second order carry out (Carry) is generated.